CBCS Scheme

USN | | | | | | | | | | |

15EC61

Sixth Semester B.E. Degree Examination, June/July 2018

Digital Communication

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Define Hilbert transform. List the properties of the Hilbert transform. **(04 Marks)**

b. Obtain the canonical representation of band pass signals. **(06 Marks)**

c. What is line coding? For the binary stream 011010 sketch the following line codes:
i) Unipolar NRZ
ii) Polar NRZ
iii) Unipolar RZ
iv) Bipolar RZ
v) Manchester **(06 Marks)**

OR

2 a. Define pre-envelope of a real valued signal. Given a band pass signal s(t), sketch the amplitude spectra of signal s(t), pre-envelope $s_+(t)$ and complex envelope $\tilde{s}(t)$. **(04 Marks)**

b. Derive the expression for the complex low pass representation of band pass systems. **(08 Marks)**

c. Write a note on HDBN signaling. **(04 Marks)**

Module-2

3 a. Explain the geometric representation of signals. Show that energy of the signal is equal to the squared length of the vector representing it. **(08 Marks)**

b. Derive the expressions for mean and variance of the correlator outputs. Also show that the correlator outputs are statistically independent. **(08 Marks)**

OR

4 a. Explain the Gram-Schmidt orthogonalization procedure. **(06 Marks)**

b. Obtain the maximum likelihood decision rule for the signal detection problem. **(10 Marks)**

Module-3

5 a. Explain the signal space representation for binary phase shift keying modulation. Also derive the expression for the probability of error for the binary phase shift keying. **(10 Marks)**

b. With a neat block diagram, explain the generation and coherent detection of QPSK signals. **(06 Marks)**

OR

6 a. With a neat block diagram, explain the non-coherent detection of binary frequency shift keying technique. **(04 Marks)**

b. Derive an expression for probability of error of binary frequency shift keying technique. Also draw the block diagrams of BFSK transmitter and coherent receiver. **(10 Marks)**

c. For the binary sequence given by 10010011, illustrate the operation of DPSK. **(02 Marks)**

Module-4

7 a. With a neat block diagram of digital PAM system obtain the expression for inter symbol interference (ISI). **(06 Marks)**

b. State and prove Nyquist condition for zero ISI. **(06 Marks)**

c. For the binary data sequence $\{d_n\}$ given by 11101001. Determine the precoded sequence, transmitted sequence, received sequence and the decoded sequence. **(04 Marks)**

OR

8 a. Explain the design of band limited signals with controlled ISI. **(10 Marks)**

b. What is a zero forcing equalizer? With a neat block diagram, explain the operation of linear transversal filter. **(06 Marks)**

Module-5

9 a. Explain the model of a spread spectrum digital communication system. **(06 Marks)**

b. Explain the generation and demodulation of direct sequence spread spectrum signals with necessary equation and block diagram. **(07 Marks)**

c. Write a note on low detectability signal transmission as an application of direct sequence spread spectrum. **(03 Marks)**

OR

10 a. With a neat block diagram, explain the frequency hopped spread spectrum. **(07 Marks)**

b. Explain the effect of despreading on a Narrow band interference in direct sequence spread spectrum systems. A direct sequence spread spectrum signal is designed to have the power ratio P_R/P_N at the intended receiver is 10^{-2}. If the desired $E_b/N_o = 10$ for acceptable performance, determine the minimum value of processing gain. **(06 Marks)**

c. Write a note on code division multiple access as an application of direct sequence spread spectrum. **(03 Marks)**

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CBCS Scheme

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15EC62

Sixth Semester B.E. Degree Examination, June/July 2018
ARM Microcontroller & Embedded Systems

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. With a neat diagram, explain the architecture of ARM cortex M3 microcontroller. **(10 Marks)**

b. Explain the register organization of Cortex M3. **(06 Marks)**

OR

2 a. Explain the operation modes and privilege levels available in ARM cortex M3 with a neat transition diagram. **(06 Marks)**

b. Mention the instructions used for accessing the special registers. Explain the same using suitable examples. **(04 Marks)**

c. Explain the stack operations using Push and Pop instructions in ARM Cortex M3. **(06 Marks)**

Module-2

3 a. Explain shift and Rotate instructions available in ARM Cortex M3 instruction set. Why is there rotate right instruction but no rotate left instruction in Cortex M3? **(08 Marks)**

b. Explain the following instructions with suitable example:
(i) BFC (ii) SXTH (iii) UBFX (iv) RBIT **(08 Marks)**

OR

4 a. Write the memory map and explain memory access attributes in Cortex M3. **(08 Marks)**

b. Analyse the following instructions and write the contents of the registers after the execution of each instruction:
Assume R8 = 0x00000088, R9 = 0x00000006 and R3 = 0x00001111
(i) RSB.W R8, R9, #0x10
(ii) ADD R8, R9, R3
(iii) BIC.W R6, R8, #0x06
(iv) ORR R8, R9 **(08 Marks)**

Module-3

5 a. Differentiate between:
(i) RISC and CISC architecture.
(ii) Little Endian and Big Endian architecture. **(08 Marks)**

b. What are the features of the following:
(i) I2C bus
(ii) IrDA
(iii) Optocoupler
(iv) 1-wire interface **(08 Marks)**

OR

6 a. What are the different types of memories used in Embedded system design? Explain the role of each. **(08 Marks)**

b. Explain the following circuits in an embedded system :

(i) Brown-out protection unit.

(ii) Reset circuit. **(08 Marks)**

Module-4

7 a. Explain the term quality attributes in an embedded system development context. What are the different quality attributes to be considered in an embedded system design. **(08 Marks)**

b. Explain Data flow graph and control data flow graph models in the embedded design. **(08 Marks)**

OR

8 a. Explain the different 'Embedded firmware design' approach in detail. **(08 Marks)**

b. Explain the characteristics of an Embedded system. **(08 Marks)**

Module-5

9 a. Explain the concept of 'deadlock' with a neat diagram. Mention the different conditions which favours a deadlock situation. **(08 Marks)**

b. Write a block schematic of IDE environment for embedded system design and explain their functions in brief. **(08 Marks)**

OR

10 a. Three processes with process IDs P_1, P_2, P_3 with estimated completion time 10, 5, 7 milliseconds respectively enters the ready queue together. A new process P_4 with estimated completion time 2 ms enters the 'Ready' queue after 2 ms. Calculate the waiting time for all the processes and the turn around time for all the processes. Also, calculate the average waiting time and average turn around time. The algorithm used is SJF (Shortest Job First) based preemptive scheduling. Assume all the process contain only CPU operation and no I/O operation are involved. **(08 Marks)**

b. Mention the sequence of operations for embedding the firmware with a programmer and draw the interfacing diagram. **(08 Marks)**

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15EC63

Sixth Semester B.E. Degree Examination, June/July 2018
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Discuss the working of nMOS enhancement mode transistor operation with neat diagrams. **(06 Marks)**

b. Explain the CMOS inverter DC characteristics highlighting the regions of operation. **(10 Marks)**

OR

2 a. With neat diagrams discuss the nMOS fabrication process steps. **(09 Marks)**

b. Explain the following :
(i) Channel length modulation
(ii) Noise Margin **(07 Marks)**

Module-2

3 a. Discuss the CMOS design style with a diagram. **(05 Marks)**

b. Draw the stick diagram for the following using CMOS logic:
(i) $Y = \overline{A + B + C}$ (ii) 2 i/p NAND gate **(05 Marks)**

c. Discuss the different contact cuts with an example to each. **(06 Marks)**

OR

4 a. With a diagram derive an expression for sheet resistance and mention the R_s values of metal, p and n transistor channels for 5 µm technology. **(05 Marks)**

b. Derive an equation for rise time and fall time with respect to CMOS inverter. **(08 Marks)**

c. Draw the circuit and stick diagram for 2 i/p NOR gate using CMOS logic. **(03 Marks)**

Module-3

5 a. Explain the constant field, constant voltage scaling models with a diagram and scaling effect table. **(06 Marks)**

b. Discuss the problems associated in VLSI design. How do you reduce them? **(05 Marks)**

c. Discuss the different bus architectures. **(05 Marks)**

OR

6 a. Discuss the design of a 4-bit adder. **(07 Marks)**

b. With relevant diagram discuss Manchester carry chain operation. **(05 Marks)**

c. Explain the carry select adder with a diagram. **(04 Marks)**

Module-4

7 a. Discuss the programmable logic array with its structure and floor plan. **(05 Marks)**

b. Discuss the architectural issues related to VLSI sub system design. **(06 Marks)**

c. Discuss the design of Data selectors. **(05 Marks)**

OR

8 a. Explain the architecture of field programmable gate array. **(10 Marks)**
b. Discuss the FPGA abstractions with a diagram. **(06 Marks)**

Module-5

9 a. Explain three transistor DRAM with its diagram and stick diagram. **(07 Marks)**
b. Discuss the ASM chart for JK flip flop with its NAND logic arrangement. **(09 Marks)**

OR

10 a. Explain logic verification process with its functional equivalence diagram. **(06 Marks)**
b. Discuss the design for manufacturability. **(06 Marks)**
c. Discuss the Ad-hoc testing. **(04 Marks)**

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15EC64

Sixth Semester B.E. Degree Examination, June/July 2018
Computer Communication Networks

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Explain the significance of layers in TCP/IP protocol suite with neat diagram. **(08 Marks)**
b. Illustrate with an example byte stuffing and bit stuffing. **(04 Marks)**
c. Explain briefly four physical topologies of a network. **(04 Marks)**

OR

2 a. Explain ARP operation and ARP packet format with a neat diagram. **(08 Marks)**
b. Describe the operation of STOP and WAIT protocol also FSM for STOP and WAIT protocol. **(08 Marks)**

Module-2

3 a. Explain the three strategies used in CSMA/CA collision avoidance. **(06 Marks)**
b. A pure ALOHA network transmits 200 bit frames on a shared channel of 200 kbps. What is the throughput if the system produces (i) 1000 frames per sec (ii) 500 frames per sec (iii) 250 frames per sec. **(04 Marks)**
c. With a neat diagram explain Ethernet frame format. **(06 Marks)**

OR

4 a. Describe persistence methods in CSMA with flow diagram. **(06 Marks)**
b. Write short notes on 10 Base 5 Ethernet and 10 Base 2 Ethernet. **(06 Marks)**
c. Describe Polling in controlled access method. **(04 Marks)**

Module-3

5 a. Explain Hidden station problem in wireless networks. **(05 Marks)**
b. Describe Spanning Tree Algorithm with an example. **(06 Marks)**
c. Explain Datagram approach in connectionless service to route the packet. **(05 Marks)**

OR

6 a. With a neat diagram describe the two kinds of services defined by wireless architecture. **(05 Marks)**
b. Explain with a neat diagram VLAN, membership and configuration of VLAN. **(06 Marks)**
c. Explain a simple implementation of Network Address Translation (NAT) and address translation with a neat diagram. **(05 Marks)**

Module-4

7 a. Explain IPV4 Datagram format. **(08 Marks)**
b. Explain with an example distance vector routing algorithm. **(08 Marks)**

OR

8 a. Explain with a neat diagram the three phases in Mobile host communication. **(08 Marks)**
b. Explain with an example link state routing and also apply Dijksthra algorithm to find least cost path tree. **(08 Marks)**

Module-5

9 a. Explain why the send window size for Go-Back N must be less than 2^m. **(05 Marks)**

b. Explain sending and receiving buffers in TCP. **(05 Marks)**

c. With a neat diagram explain TCP segment format. **(06 Marks)**

OR

10 a. Explain why the size of the send and receiver window in selective repeat can be atmost one half of 2^m. **(05 Marks)**

b. Discuss the general services provided by UDP. **(05 Marks)**

c. Explain with a neat diagram connection establishment using three way handshaking in TCP. **(06 Marks)**

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15EC654

Sixth Semester B.E. Degree Examination, June/July 2018
Digital Switching Systems

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing one full question from each module.***

Module-1

1 a. Explain in detail with a neat diagram of different network structures. **(08 Marks)**

b. Draw a neat diagram of four-wire circuit and explain its working. **(08 Marks)**

OR

2 a. Differentiate between TDM and FDM transmission network, with suitable diagrams. **(08 Marks)**

b. Explain in details PDH and SDH with neat diagrams. **(08 Marks)**

Module-2

3 a. Explain in brief distributed systems with neat diagrams. **(08 Marks)**

b. Explain different functions of switching systems. **(08 Marks)**

OR

4 a. Explain in detail building blocks of a digital switching of system. With neat block diagrams. **(08 Marks)**

b. Explain in brief basic call processing with diagrams. **(08 Marks)**

Module-3

5 a. Define the following:
(i) Busy hour (ii) Grade of service (iii) Holding time
(iv) Statistical equilibrium **(08 Marks)**

b. Derive an expression for the second Erlang's distribution starting from basic principles. **(08 Marks)**

OR

6 a. Design a progressive grading system connecting 20 outgoing trunks and having a switch with availability of 10. Draw the grading diagram. **(08 Marks)**

b. Design a three stage network for 100 incoming trunks to 400 outgoing trunks. Draw the diagram. **(08 Marks)**

Module-4

7 a. With a neat sketch, explain space switch in detail. **(08 Marks)**

b. Explain in brief frame alignment with neat sketch. Explain different types of synchronization networks. **(08 Marks)**

OR

8 a. With a neat diagram, explain Level 1, Level 2 and Level 3 control of a digital switching system. **(08 Marks)**

b. What is feature flow diagram? Draw feature flow diagram for feature activation, feature operation and feature deactivation for a call forwarding feature. **(08 Marks)**

Module-5

9 a. Explain the interface of digital switching central office with neat diagram. **(08 Marks)**

b. Highlight the strategy for improving software quality. **(08 Marks)**

OR

10 a. Explain generic switch software and hardware architecture. With respect to suitable diagram. **(08 Marks)**

b. Explain recovery stage of initialization process with examples. **(08 Marks)**

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CBCS SCHEME

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15EC663

Sixth Semester B.E. Degree Examination, June/July 2018
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. What are the two sources of power consumption in digital components? Explain. **(04 Marks)**

b. Develop a verilog model for a 4 : 1 multiplexer. **(04 Marks)**

c. Design an encoder for the buglar alarm that has sensors for each of the 8 zones as a priority encoder with zone 1 having highest priority down to zone 8 having lowest priority. **(08 Marks)**

OR

2 a. Explain the simple design methodology followed in IC industry. **(08 Marks)**

b. Develop a datapath to perform complex multiplication of two complex number whose real and imaginary parts are represented as signed fixed point numbers with 4-pre binary points and 12 post-binary points. Real and imaginary parts of the product are represented with 8 pre-binary points and 24 post-binary points. Area is the main constraint. Also write the verilog model of the complex multiplier datapath. **(08 Marks)**

Module-2

3 a. Design a $1m \times 8$ bit composite memory using 512 K $\times 8$ bit memory component. **(04 Marks)**

b. Design a $16K \times 48$ – bit memory using $16K \times 16$ – bit memory component. **(04 Marks)**

c. Explain flowthrough and pipelined SSRAM with the help of timing diagram. **(08 Marks)**

OR

4 a. Determine whether there is an error in the ECC word 000111000100 and if so, correct it. **(06 Marks)**

b. Develop a verilog model of a dual – port $4K \times 16$ bit flow through SSRAM. One port allows data to be written and read, while the other port allows data to be read. **(06 Marks)**

c. Explain dynamic RAM operation. **(04 Marks)**

Module-3

5 a. Write and explain the internal organization of a CPLD. **(08 Marks)**

b. What are the two main design and manufacturing techniques for ASIC's. Explain. **(08 Marks)**

OR

6 a. Write and explain the internal organization of FPGA. **(08 Marks)**

b. Explain differential signaling in detail. **(08 Marks)**

Module-4

7 a. Explain Flash ADC and successive approximation ADC with the help of necessary diagrams. **(08 Marks)**

b. Design an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the I/P value changes. The controller is the only interrupt source in the system. Also develop a verilog model of the I/P controller. **(08 Marks)**

OR

8 a. Explain the following serial interface standards for connecting I/O devices:
(i) I^2C (ii) USB **(08 Marks)**

b. With a neat diagram, explain R-string DAC and R/2R ladder DAC. **(08 Marks)**

Module-5

9 a. Explain the design flow of hardware/software co-design. **(10 Marks)**

b. Explain floorplan, placement and routing of ASIC physical design. **(06 Marks)**

OR

10 a. Explain Built-In Self Test (BIST) techniques. **(08 Marks)**

b. Explain the terms scan design and boundary scan. **(08 Marks)**

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